WHAT IS CLAIMED IS:

1. A method for creating semiconductor transistor devices on a silicon-on-insulator (SOI) structure including a buried oxide (BOX) layer and an active layer above the BOX layer, the method comprising:

implanting n-type or p-type dopants into the active layer to create n-wells or p-wells respectively and so as to form device regions in the active layer;

forming gate stacks on the device regions so as to define underlying channel regions;

implanting dopants into the n-wells or p-wells so as to form source and drain regions such that the gate stacks substantially inhibit penetration of the dopants into the channel regions;

forming a masking layer with openings at least partially over the gate stacks and so as to mask remaining regions of the SOI structure not underlying the gate stacks;

implanting first additional dopants through the openings such that the additional dopants come to reside within the BOX layer underlying the channel regions so as to create localized borophosphosilicate glass (BPSG) diffusion sources within the BOX layer;

implanting second threshold adjust dopants into the n-wells and p-wells to change a threshold voltage of the resulting transistor devices; and

processing the SOI structure so as to induce the diffusion sources to establish retrograde dopant profiles in the channel regions having a peak concentration near the BOX.

2. The method of Claim 1, wherein the openings of the mask layer are grouped to overlie only a portion of the SOI structure.

3. The method of Claim 2, wherein the openings are formed to overlie a central portion of the SOI structure and openings are not formed in a peripheral portion of the SOI structure.

4. The method of Claim 2, comprising forming a first set of the transistor devices adjacent the openings and defining an array of memory cells having a first set of transistor

device characteristics and forming a second set of the transistor devices not underlying the openings defining peripheral logic access and control circuits having a second set of device characteristics.

5. The method of Claim 4, wherein the memory cells comprise DRAM cells.

6. The method of Claim 1, wherein processing the SOI structure so as establish the retrograde dopant profiles comprises forming a passivation layer with attendant high temperature processing.

7. The method of Claim 1, wherein the second threshold adjust dopants are implanted before forming the masking layer.

8. The method of Claim 1, wherein the second threshold adjust dopants are implanted through the openings in the masking layer.

9. The method of Claim 1, wherein the openings are formed to be asymmetric with respect to the source and drain regions such that asymmetric diffusion sources and asymmetric retrograde dopant profiles are formed.

10. The method of Claim 9, wherein the asymmetric, retrograde dopant profiles define asymmetric device characteristics for the transistor devices.

11. A method for creating semiconductor transistor devices on a silicon-on-insulator (SOI) structure including a buried oxide (BOX) layer and an active layer above the BOX layer, the method comprising:

implanting n-type or p-type dopants into the active layer to create n-wells or p-wells respectively and so as to form device regions in the active layer;

forming gate stacks on the device regions so as to define underlying channel regions;

implanting dopants into the n-wells or p-wells so as to form source and drain regions such that the gate stacks substantially inhibit penetration of the dopants into the channel regions;

forming a masking layer with asymmetric openings at least partially over the gate stacks and so as to mask remaining regions of the SOI structure not underlying the gate stacks;

implanting first additional dopants through the openings such that the additional dopants come to reside within the BOX layer underlying the channel regions so as to create asymmetric borophosphosilicate glass (BPSG) diffusion sources within the BOX layer; and

processing the SOI structure so as to induce the diffusion sources to establish asymmetric retrograde dopant profiles in the channel regions having a peak concentration near the BOX.

12. The method of Claim 11, wherein the openings of the mask layer are grouped to overlie only a portion of the SOI structure.

13. The method of Claim 12, wherein the openings are formed to overlie a central portion of the SOI structure and openings are not formed in a peripheral portion of the SOI structure.

14. The method of Claim 12, comprising forming a first set of the transistor devices adjacent the openings and defining an array of memory cells having a first set of transistor device characteristics and forming a second set of the transistor devices not underlying the openings defining peripheral logic access and control circuits having a second set of device characteristics.

15. The method of Claim 14, wherein the memory cells comprise DRAM cells.

16. The method of Claim 11, wherein processing the SOI structure so as establish the asymmetric retrograde dopant profiles comprises forming a passivation layer with attendant high temperature processing.

17. The method of Claim 11, further comprising implanting second threshold adjust dopants into the n-wells and p-wells to change a threshold voltage of the resulting transistor devices.

18. The method of Claim 17, wherein the second threshold adjust dopants are implanted before forming the masking layer.

19. The method of Claim 17, wherein the threshold adjust dopants are implanted through the openings in the masking layer.

20. The method of Claim 11, wherein the asymmetric, retrograde dopant profiles define asymmetric device characteristics for the transistor devices.

21. A method for creating semiconductor transistor devices on a silicon-on-insulator (SOI) structure including a buried oxide (BOX) layer and an active layer above the BOX layer, the method comprising:

implanting n-type or p-type dopants into the active layer to create n-wells or p-wells respectively and so as to form device regions in the active layer;

forming gate stacks on the device regions so as to define underlying channel regions;

implanting dopants into the n-wells or p-wells so as to form source and drain regions such that the gate stacks substantially inhibit penetration of the dopants into the channel regions;

forming a masking layer with openings at least partially over the gate stacks and so as to mask remaining regions of the SOI structure not overlying the gate stacks;

implanting first additional dopants through the openings such that the additional dopants come to reside within the BOX layer underlying the channel regions so as to create borophosphosilicate glass (BPSG) diffusion sources within the BOX layer; and

processing the SOI structure so as to induce the diffusion sources to establish retrograde dopant profiles in the channel regions having a peak concentration near the BOX.

22. The method of Claim 21, wherein the openings of the mask layer are grouped to overlie only a portion of the SOI structure.

23. The method of Claim 22, wherein the openings are formed to overlie a central portion of the SOI structure and openings are not formed in a peripheral portion of the SOI structure.

24. The method of Claim 22, comprising forming a first set of the transistor devices adjacent the openings and defining an array of memory cells having a first set of transistor device characteristics and forming a second set of the transistor devices not underlying the openings defining peripheral logic access and control circuits having a second set of device characteristics.

25. The method of Claim 24, wherein the memory cells comprise DRAM cells.

26. The method of Claim 21, wherein processing the SOI structure so as establish the retrograde dopant profiles comprises forming a passivation layer with attendant high temperature processing.

27. The method of Claim 21, further comprising implanting second threshold adjust dopants into the n-wells and p-wells to change a threshold voltage of the resulting transistor devices.

28. The method of Claim 27, wherein the second threshold adjust dopants are implanted before forming the masking layer.

29. The method of Claim 27, wherein the threshold adjust dopants are implanted through the openings in the masking layer.

30. The method of Claim 21, wherein the openings are formed to be asymmetric with respect to the source and drain regions such that asymmetric diffusion sources and asymmetric retrograde dopant profiles are formed.

31. The method of Claim 30, wherein the asymmetric, retrograde dopant profiles define asymmetric device characteristics for the transistor devices.

32. A semiconductor transistor device comprising:

a semiconductive substrate;

an insulative layer buried within the semiconductive substrate;

an active layer of semiconductive material above the insulative layer;

a gate structure formed on the active layer; and

source and drain regions formed in the active layer wherein the insulative layer is provided with a dopant diffusion source localized under the gate structure between the source and drain regions and wherein the dopant diffusion source is diffused into the active layer so as to define a retrograde dopant profile in the active layer under the gate stack substantially between the source and drain regions.

33. The device of Claim 32, wherein the retrograde dopant profile has a peak concentration substantially adjacent the interface of the insulative layer and the active layer.

34. The device of Claim 32, wherein the retrograde dopant profile provides the transistor device with improved resistance to drain-induced barrier lowering (DIBL).

35. The device of Claim 32, wherein the retrograde dopant profile in the active layer is asymmetrically positioned with respect to the source and drain regions.

36. The device of Claim 32, wherein the active layer further comprises threshold adjust dopants positioned substantially between the source and drain regions and under the gate structure.

37. The device of Claim 32, wherein the insulative layer with dopant diffusion source comprises borophosphosilicate glass (BPSG).

38. A method for creating semiconductor transistor devices on a silicon-on-insulator (SOI) structure including a buried oxide (BOX) layer and an active layer above the BOX layer, the method comprising:

implanting n-type or p-type dopants into the active layer to create n-wells or p-wells respectively and so as to form device regions in the active layer;

forming gate stacks on the device regions so as to define underlying channel regions;

implanting dopants into the n-wells or p-wells so as to form source and drain regions such that the gate stacks substantially inhibit penetration of the dopants into the channel regions;

implanting first additional dopants through the gate stacks such that the additional dopants come to reside within the BOX layer underlying the channel regions and substantially between the source and drain regions so as to create borophosphosilicate glass (BPSG) diffusion sources within the BOX layer; and

processing the SOI structure so as to induce the diffusion sources to establish retrograde dopant profiles in the channel regions having a peak concentration near the BOX.

39. The method of Claim 38, further comprising forming a masking layer with openings at least partially over the gate stacks and so as to mask remaining regions of the SOI structure not overlying the gate stacks and wherein implanting the first additional dopants through the gate stacks comprises implanting the first additional dopants through the openings.

40. The method of Claim 39, wherein the openings are formed to be asymmetric with respect to the source and drain regions such that asymmetric diffusion sources and asymmetric retrograde dopant profiles are formed.

41. The method of Claim 40, wherein the asymmetric, retrograde dopant profiles define asymmetric device characteristics for the transistor devices.

42. The method of Claim 38, wherein processing the SOI structure so as establish the retrograde dopant profiles comprises forming a passivation layer with attendant high temperature processing.

43. The method of Claim 38, further comprising implanting second threshold adjust dopants into the n-wells and p-wells to change a threshold voltage of the resulting transistor devices.

44. The method of Claim 43, wherein the second threshold adjust dopants are implanted through the gate stacks.